Nitron

Nitrochip

SEMI-CUSTOM GATE-ARRAY PRODUCTS

- CMOS METAL GATE
- CMOS SILICON GATE – HIGH PERFORMANCE

1982

NITROCHIP - SEMI CUSTOM GATE ARRAY

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NITRON OVERVIEW

Nitron is a high technology corporation involved in the design and manufacturing of large scale integrated circuits including standard, custom, and semi-custom. Since its inception the company has stressed technological innovation in both manufacturing capabilities and its products.

Nitron utilizes a variety of processes including n-channel, p-channel, CMOS, and a state-of-the-art MNOS (Metal Nitride Oxide Silicon) capability to help maintain a competitive edge in its product line. The unique non-volatile memory (NVM) technology led to the introduction of Nitron's nonvolatile Electrically Alterable Read-Only Memory (EAROM). EAROMs combine the non-volatility of a ROM with the in-circuit alterability of a RAM.

The company was founded in 1972 as a captive supplier for McDonnell Douglas Corporation. Nitron became a division of that corporation in 1976, with worldwide sales of its LSI semiconductor products. In December 1977, Nitron became a wholly-owned subsidiary of Nanon Electronics, Inc. of Cupertino, California. In April 1980, Nitron and Nanon merged their respective operations and became known as Nitron, Inc., operating as a privately held firm, largely employee owned.

On May 27, 1980, Nitron Inc., filed with the Securities and Exchange Commission to offer stock for sale to the public. Nitron, Inc. is now a public company.

NITRON'S PLACE IN THE INDUSTRY

Nitron is committed to vigorous participation in the multi-billion dollar electronic communications market, a spectrum which includes the transmission of signals or information carrying data, video, and/or voice. In this market segment, mechanical parts are being replaced by semiconductor components in a dramatic manner. This market, which is estimated to grow from approximately $60 billion in 1980 to $190 billion by 1990, includes automotive, computer, consumer, industrial and instrumentation for all kinds of applications.

Our technology niche is one that we feel will have significant impact in the industry. Nitron was one of the first companies involved in the development of non-volatile memories (NVM).

NVM technology permits the storage of information after power is removed for any reason. This ability to retain memory has important applications in a wide range of products including a host of energy saving devices.

In the process niche, we at Nitron are emphasizing the CMOS process:

mature, high yielding metal-gate and a new high performance CMOS silicon gate. Nitron elected to enter into this advanced technology because of the lower power consumption of CMOS technology. Less power means that more devices can be integrated on a single chip without performance becoming adversely impacted by heat generation. These process technologies are used in the Nitrochip semi-custom product line.

Nitron's 50,000 square foot facility is completely integrated providing the capability to bring products from concept through development and into cost-effective manufacturing. Various facilities and assets routinely utilized at Nitron to accomplish this include computer-aided design (CAD), mask making, wafer fab, and assembly. Well established quality and reliability assurance programs are in place for industrial, consumer and military product requirements.

Combined with offshore assembly facilities, Nitron is able to provide the customer with his high volume requirements while maintaining the responsiveness and dedication to quality that has contributed to the company's growth.

The firm has in-house facilities and equipment to perform all wafer fab steps, assembly, and testing. Nitron fabricates its tooling in its own mask shop to allow fast cycle times for generating masks. The mask plates are produced from rubylith artwork or from pattern-generated (P.G.) reticle tapes. The facility also contains an assembly area for ceramic and cerdip packages capable of producing 10,000 units per week.

Nitron owns a laser-controlled step-and-repeat camera. Its mask-making equipment is capable of producing 3-, 4-, and 5-inch plates. In wafer processing, it operates 48 diffusion tubes capable of processing 3-inch and 4-inch wafers. The company owns a 200KV ion implanter, 3 Sentry 600 automated test systems, and an International Plasma System Corp. Model 2000 wafer etcher.

The company has design and process know-how to fabricate both custom and standard products in PMOS, NMOS, CMOS, both metal-and silicon-gate technologies. Nitron is one of a handful of semiconductor firms with a capability to manufacture non-volatile memories. Its ion implant capability includes implants of boron, phosphorus, and arsenic at voltages up to 200KV. Ion implants allow the adjustment of transistor thresholds, creation of depletion-mode transistor loads, and changes to supply voltages.

The Nitron Difference

As a semi-custon gate array supplier, Nitron offers a combination of capabilities unique in this class of products

- o Fully facilitized in one facility for engineering, design, mask making, wafer fab, ion implant, assembly, and test
- o Established CMOS production processes
- o Established capability to build and inspect for Mil Std 883 criteria and meet full military environment.
- o Simulation and fault inspection techniques to insure high reliability products
- o Non volatile memory product base for companion dévices
- o Full custom design/fab capability when economics dictate conversion from semi-custom to custom.

SEMI-CUSTOM DESIGN CONCEPT

Traditionally, the development of custom ICs has been a long and costly undertaking; the development time would normally run in excess of one year, design changes are slow and costly, and it may take a long time to get from prototype to full production. Because of these difficulties, the use of custom ICs could be economically justified only when a very large quantity of circuits; i.e., several hundred-thousand or more units, were required during the life of the end product. In the past, these drawbacks have severely limited the use of custom monolithic ICs.

The semi-custom design concept now overcomes this traditional problem. Nitron makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection which metallizes all selected components together in the required circuit configuration. This enables an engineer to design a metal mask based on his circuit which will interconnect the uncommitted components on the prefabricated wafers, and thus convert them into customized chips corresponding to the customer's design.

The Nitrochip concept is a unique approach to the design and manufacture of custom integrated circuits, where every step in the process is optimized for low volume custom IC production. Each Nitrochip circuit is a predesigned and pre-processed array of circuit elements, ready to be interconnected into a custom integrated circuit for each special requirement.

Since only one mask layer needs to be customized for each circuit, development costs are minimized and the development schedule is much shorter than for a fully custom design.

The semi-custom program is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks, at approximately 10% to 20% of the development of tooling costs associated with the conventional full custom design. The semi-custom design concept is an inter-active or cooperative development effort between Nitron and the customer. In most cases, the cost and the development time for the program can be reduced even further by having the customer do the design and breadboarding of his own semi-custom IC, using Nitron's design manual and layout aids.

The semi-custom design approach is based on a number of standardized IC chips with fixed component locations. These standardized IC chips, called Nitrochips, contain a large number of undedicated active and passive components (i.e., transistors, resistors, logic gates, etc.). These integrated components can be interconnected in thousands of different ways, with a customizing interconnection pattern. Each different metal interconnection pattern creates a new custom IC. This method is called semi-custom, rather than full custom since only the last layer of tooling is changed to customize an IC chip, and the rest of the layers are standard. As a result, the development phase is very short, far less expensive and risk-free, compared to conventional full- or dedicated-custom ICs. Similarly, if a design change or iteration is necessary, it can be readily accommodated, within a matter of weeks, by simply generating a new or modified interconnection pattern.

Nitron offers two families of Nitrochips for semi-custom designs: The 5XXX, CMOS metal gate, providing seven gate sizes, from 50 to 600 gates, and the 9XXX CMOS silicon gate, providing six gate sizes, from 360 to 1600 gates, along with very high performance. The details of each of these chips are discussed in the later sections of this brochure.

NITROCHIP DESIGN - GETTING STARTED

Your very first step, at the start of the semi-custom program, should be to contact Nitron for a preliminary analysis and discussion of your needs. This initial review by Nitron is performed at no cost to the customer. Yet is is essential to the success of the program since it avoids any possible design pitfalls or misunderstandings. This early interaction also allows you to find out some of the options or variations available in Nitron's semi-custom programs and choose the one which is best suited to your needs.

The following is a typical check list of items and information which will help Nitron's technical staff to provide you with an accurate feasibility study of your project along with a quote on development costs, time tables and production pricing.

- A block diagram of circuit function, and input/output interface requirements.
- A circuit schematic or logic diagram of your circuit.
- Preliminary or objective performance specifications, limits on critical parameters (also possible tradeoffs which may be allowed).
- Types of electrical testing required for production units, (i.e., AC or DC parametric testing, functional testing, etc.)
- Production quantity requirements.
- Desired development and production timetables.
- An indication of how much of the breadboarding, layout, etc. can be done by you the customer.

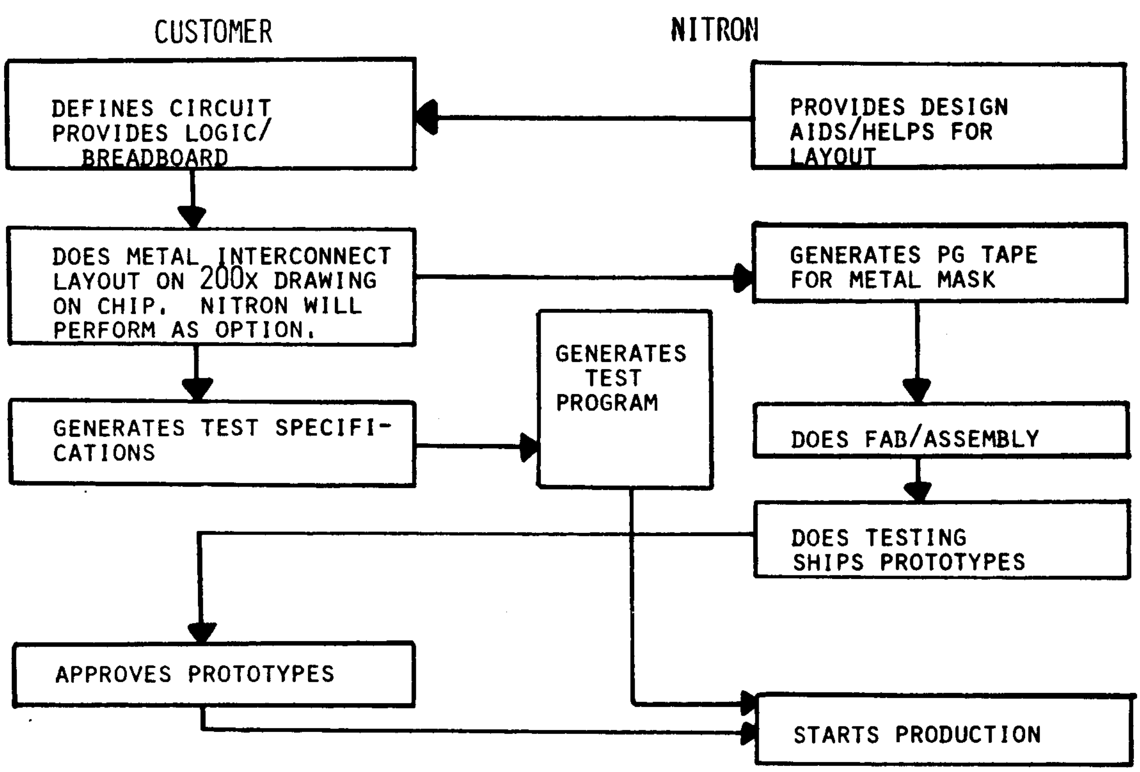
DESIGNING A NITROCHIP

Developing a new Nitrochip is a joint effort which combines your circuit design work with circuit integration skills and equipment.

The essential elements of the design process are shown in the flow below. The first step is customer definition of the circuit requirement, backed up by breadboarding and verifying circuit function, using TTL or 4000 series CMOS ICs. Typically, the customer then lays out the metal interconnect pattern on a 200X worksheet by Nitron, using techniques defined in Nitron's design manual. Should the customer lack the time or expertise for this step, Nitron will do the layout at slight extra charge.

After your layout is completed, we check it and then use it to generate an accurate 200X enlargement of your custom IC. This enlargement is then converted by Nitron into the metal mask. Using this mask, Nitrochip wafers are etched to produce the correct interconnect pattern. Finished wafers are probed and die-sorted using test programs developed jointly. Chips are mounted in cerdip packages and six to ten weeks after your schematic is received, Nitron will deliver prototypes of your integrated circuit. Small scale production can be delivered eight weeks after prototype approval ramping to full scale production deliveries (to 10,000 pcs./month) in four weeks.

TYPICAL PROGRAM FLOW



QUESTIONS AND ANSWERS

1. Development Philosophy

   A. How much does it cost to have a Nitrochip IC developed by Nitron?

   The cost for the design ranges from $5,000 to $20,000 depending on the complexity and difficulty of the design and the follow-on production. An average development cost is $10,000. If you submit a description of your requirements, Nitron will respond with a firm, fixed price quotation.

   B. What risk do we take in designing an IC ourselves?

   The design of a Nitrochip IC is no more difficult than the design of a discrete component circuit. However, a monolithic IC almost always requires differences in design approach. If, after reading the design manual, your engineers find it difficult to generate the design, Nitron will make its applications engineering available at no charge. Additionally, if requested, Nitron will perform the design for a nominal charge.

   C. What if additional design cycles are needed?

   Upon evaluation of the initial prototypes, if the customer desires to modify the design or the layout, a design interation cycle can be completed within six to ten weeks.

   Typical costs of additional design cycles are $1,200 to $2,500 plus the costs of additional prototypes supplied at the completion of the design iteration cycle.

   D. What is the development time?

   In the case of semi-custom development programs, typical development time is eight to fourteen weeks, starting with receipt of your logic schematic and ending with the delivery of 25 prototypes.

   E. What is the cost of the development program?

   The cost of the semi-custom development program depends upon several factors, including gate utilization, speed requirement, number of package pins and of course, the point at which Nitron enters the design cycle. Recent experience indicates a growing preference by users to have Nitron perform the chip layout from the user supplied schematic (which has been successfully breadboarded) and test specification. Under these conditions Nitron, alone, is responsible for the delivery of working parts.

   Under these circumstances, the basic development costs are in the range of $10,000 to $15,000, depending on the layout complexity and the particular Nitrochip used. This development cost also includes 25 monolithic prototypes. Additional prototypes are available at a nominal cost, in minimum lots of 100 units each.

2. Production Quantity

A. What quantity should I have for the Nitrochip?

If you use 5,000 circuits or more per year, the Nitrochip will definitely offer advantages. Under some circumstances, smaller production volumes will be cost effective as well, depending upon the application.

B. At what point does it become of advantage to switch to a conventional custom IC?

This depends on the percentage of components used on the Nitrochip as well as package size. For the average 80% filled Nitrochip, there is little advantage to switching to custom up to at least 100,000 pieces per year.

C. Can we negotiate an annual purchase contract?

Most Nitrochip ICs are purchased under annual, blanket purchase orders. The minimum release quantity should be 1,000 pieces and a schedule with releases for a 90-day period must be part of the order.

D. What about production pricing?

The production pricing of Nitrochips depends on a number of important factors such as:

1) Circuit complexity (i.e., yield)
2) Device performance and test requirements
3) Special environmental screening requirements (burn-in, hermeticity tests, etc.)
4) Package type required
5) Volume

Typical price ranges for the 5XXX metal gate Nitrochip family are shown below.

TYPICAL PRODUCTION PRICING, COMMERCIAL REQUIREMENT

DEVICE	SIZE	PACKAGE PINS	VOLUME LOW	VOLUME HIGH
NC5100	100 Gates	16	$ 3.50	$2.00
NC5150	150 Gates	18	$ 5.00	$2.75
NC5200	200 Gates	24	$ 7.00	$4.15
NC5350	200 Gates +32 FF	28	$ 9.00	$6.75
NC5500	450 Gates +24 FF	40	$11.00	$8.00
NC5600	350 Gates +72 FF	40	$12.00	$8.50

Pricing for the 9XXX silicon gate family is comparable on a per gate basis.

3. Production Delivery

How long does it take to get production quantities?

For quantities of less than 1000 pieces, Nitron offers an eight-week maximum lead time. Larger quantities require no more than twelve weeks.

4. Economy

How does the Nitrochip cost compare with that of a discrete component/standard IC assembly?

With very few exceptions, the Nitrochip is dramatically less expensive. This difference is especially obvious when assembly cost, P.C. board differences, stocking costs, re-work time, inspection, and testing time are included.

To illustrate this point, refer to the table below which illustrates the dependence of system costs on the number of ICs in the system.

DIGITAL SYSTEM COSTS THAT ARE PROPORTIONAL TO THE NUMBER OF ICs

PC Board	$20/board	50/board	$0.40
PC Connector	$5/board	50/board	0.10
Subrack (metalwork, guides, labor)	$200/subrack	1000/subrack	0.20
Backplane (subrack ground-power plane)	$100/subrack	1000/subrack	0.10
Wire wrap (automatic)	6¢/wire	1/wire	0.06
Power supplies ($1/W, 70% utilized)	$1.50/W	10/W	0.15
Rack (including doors, fans, power distributor)	$500/rack	4000/rack	0.13
IC ordering, receiving and inventory	2¢/IC	1	0.02
IC Testing	8¢/IC	1	0.08
PC board testing	$5/board	50/board	0.10
System checkout	$800/rack	4000/rack	0.20
Bypass capacitors (including insertion labor)	$1/board	50/board	0.02
IC insertion and soldering	6¢/IC	1	0.06
Interconnecting cables	$80/rack	4000/rack	0.02
Maintenance panel	$300/rack	4000/rack	0.07
System assembly	$200/rack	4000/rack	0.05
System packing and shipment	$200/rack	4000/rack	0.05
System design, drafting and prototype checkout (+ 100 systems)	$2000/rack	4000/rack	0.50
Service cost for 5 years	$4000/rack	4000/rack	1.00
Total Overhead Cost per IC		=	$3.31

For this rather typical example, the total overhead cost per IC is seen to be $3.31. This is in addition to the cost of the IC itself. If for example, one semi-custom chip costing $3.00 replaces 10 ICs, each of which costs $0.20, the relative costs are $6.31 for the semi-custom approach vs. $35.10 for the 10 IC approach; a rather dramatic savings at the system level.

The moral is "Rather than comparing the direct material costs at the IC level, look at the overall system cost to arrive at the real savings from semi-custom chips."

5. What about testing of semi-custom ICs?

   The initial prototypes supplied to the customer at the conclusion of the basic semi-custom program are not electrically tested. However, upon evaluation of these prototypes and the definition of test specifications by the customer, Nitron will develop test software and fixtures to provide fully tested production ICs. All production ICs. All production devices receive 100% electrical test and screening to a mutually agreed to device specification. In addition to complete electrical testing, all of the production devices are screened by Nitron's Quality Assurance Department to assure compliance with the agreed-upon Acceptable Quality Level (AQL) Standards.

   There is normally a non-recurring engineering charge associated with this test system generation, to cover the cost of the test fixture and the computer software development. Depending on the complexity of the test requirements, this test engineering charge is normally in the range of $3000 to $6000.

6. What package types are available?

   All semi-custom ICs are available in dual-in-line (DI) packages. Commercial grade units are normally packaged in plastic DIP packages. Nitron offers a wide selection of such packages in 8-, 14-, 16-, 18-, 20-, 24-, 28-, and 40-pin versions. Industrial or military grade products requiring hermetic packaging are available in fritseal ceramic (CERDIP) and/or side brazed ceramic packages. All of the packaged units are subjected to Nitron's stringent Quality Assurance specifications prior to shipment. Other package types can be specified, including flat packs and leadless chip carriers.

7. Is there a second-source for semi-custom ICs?

   In most high-volume production applications of ICs, the customer often requires more than one supplier of a given IC. Anticipating this "alternative-source" requirement, Nitron contractual agreements with qualified second sources for each of the Nitrochip families. For the metal gate, 5XXX family, the second source is Master Logic of Sunnyvale, California. For the 9XXX silicon gate family, the second source is Universal Semiconductor, of San Jose, California.

In addition, where a critical supply situation may exist, Nitron can also provide a special "bonded inventory" of parts, either in chip form or in packaged form, with prior arrangement with the customer.

8. Can Nitron supply unpackaged die?

   All of Nitron's semi-custom products can be supplied in die form, for hybrid assemblies.

9. Can Nitron do environmental screening?

   Nitron has complete burn-in, environmental test and screening services available for temperature-stressing, thermal-shock or humidity and hermeticity tests. For a detailed analysis of your needs, consult Nitron's Marketing Department.

10. What if my production requirements exceed my initial expectations?

    It is not unusual for an end-product using the semi-custom IC to be extremely successful in a very short time. In that case, the anticipated volume of the custom IC may jump from few thousand units to several hundred-thousand units. When that happens, Nitron can quickly convert your semi-custom design to a full custom chip and make it much more cost-effective for you. Translating a semi-custom design to a full custom IC is a relatively simple trouble-free step, which can be normally done is less than six months and at a modest cost.

11. Secrecy

    What proprietary protection do we have?

    Any information submitted by you is held in confidence. The interconnection mask generated for your circuit is your exclusive property. Nitron will not sell your Nitrochip IC to anybody else without your written permission.

12. Warranty

    The customer has 30 days to reject product based on incoming acceptance criteria. Otherwise the Nitrochip is warranted for one year from delivery to be free of defects, in accordance with Nitron's standard warranty policy.

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

Nitron is now able to offer you the advantages of semi-custom and full custom design programs because of our in-house complete semiconductor manufacturing capability. This unique capability gives us the ability to start a custom development program using a combination of our semi-custom Nitrochips during the initial or early phases of a customer's product, taking full advantage of the low tooling cost and short development cycle. As a customer's product matures and its market expands, resulting in higher volume production run custom IC, achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced; the IC design approach has been proven, production "bugs" are out of your product and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC system in your product can be phased-out while the full custom IC is being phased-in.

Nitron's unusual capability of combining both full and semi-custom design capabilities and a complete wafer fabrication capability under one roof uniquely provides for initially developing the prototypes in a semi-custom form, and then converting them to full custom. In this manner, the customer has the "best of two worlds" in utilizing the combination of these two technologies: the quick turnaround advantages of semi-custom Nitrochips provide prototypes and the initial production units; the subsequent full custom design provides cost savings at high volume production. Yet, during this transition, the customer is assured of a continuous flow of product through is production line.

In addition to allowing the cost advantage of early production, in such a "Two-Step" development, the semi-custom prototypes often serve as a "monolithic breadborad" to optimize and de-bug the final design. The performance of the semi-custom chip accurately simulates the characteristics of the final, full custom design. Yet, it allows one to perform design iterations or changes in a very efficient and cost-effective form. In fact, the only difference between the semi-custom and the full custom chip is the actual "size" of the silicon chip.

Once the design is satisfactory, conversion of a semi-custom to a full custom chip is very straight forward and relatively risk free: we simply remove the unused electrical components from the chip to reduce the chip size and pass the resulting cost savings to you in the form of reduced unit price.

The "Two-Step" development capability, i.e., start as semi-custom and finish as full custom, is a very powerful design technique. It avoids the risks associated with a conventional "black box" type custom design where one doesn't know, until the very last day of development, whether the circuit works or it is manufacturable.

Since it avoids costly design iteration or modification cycles, the "Two-Step" program does not take any longer or cost more than the conventional full custom development; yet it gives one a very high degree of assurance that the final custom unit will "work the first time".

FEATURES OF CMOS TECHNOLOGY

Some of the features of CMOS technology which make it attractive for semi-custom LSI implementation are the following:

- All CMOS logic circuits can be constructed from a few circuit elements. This feature allows a very wide variety of logic circuits to be constructed from each CMOS monochip.
- Well-defined logic levels; the two logic levels in CMOS are the positive and negative supply voltage.
- Wide tolerance of operation; CMOS circuit typically operate over a supply voltage range from 3 volts to 15 volts and from -55°C to +125°C with no change in operation except circuit delay, which varies in a predictable manner, and power supply current drain.
- Ease of breadboarding; numerous standard parts are available, including a very wide selection of MSI functions.
- Reliability history; CMOS processing has stabilized and a large body of reliability data has accumulated on CMOS circuits.
- Ease of interface; CMOS elements can be configured to match the input or output requirements of most standard logic familites, and can interface with many unique circuit elements such as relays and displays.
- Low power operation; one of the most attractive features of CMOS logic is the very low quiescent power, which makes CMOS logic a natural choice for battery operated applications.
- Easy conversion to full custom when volume justified.
- Potential for analog and digital functions on the same chip.

DESCRIPTION OF NITROCHIP ORGANIZATION

Each Nitrochip device contains a number of cells of differing types as follows:

Device Cells	-	Basic internal gate building blocks - each one
Driver Cells	-	Low impedance cells intended for ouptput driver
Buffer Cells	-	Design for input cooling
Hi Temperature Cells	-	Used as hi impedance circuit elements; i.e., pull up device
Corner Cells	-	Test devices for process monitoring

The logic function capability of a device cell is tabulated as follows:

Function	No. Of Device Cells
2 Inverter	½
2.3 in gate	1
Transmission gate	½
Exclusive OR	2
Schmidt Trigger	3
Set-Reset FF	2
D Flip Flop	4
JK Flip Flop	6

Nitron's Nitrochip product family, showing gate equivalents and cell configuration may now be tabulated.

Nitrochip Gate Array Families

5XXX Metal Gate

DEVICE TYPE	EQUIVALENT TWO INPUT GATE	DRIVER CELLS	BUFFER CELLS	DEVICE CELLS	BONDING PADS
NC5050	50	10	18	22	22
NC5100	100	14	15	56	32
NC5150	150	18	16	81	38
NC5200	200	18	22	108	44
NC5350	200 + 32 FF	16	30	112	53
NC5500	450 + 24 FF	20	42	232	84
NC5600	350 + 72 FF	20	42	184	84

9XXX Silicon Gate

DEVICE TYPE	EQUIVALENT TWO INPUT GATE	DEVICE CELLS	I/O CELLS	BONDING PADS
NC9360	360	360	50	50
NC9540	540	540	60	60
NC9720	720	720	68	68
NC9960	960	960	78	78
NC91200	1200	1200	86	86
NC91500	1500	1500	96	96

AVAILABLE IN PLASTIC, CERDIP, OR CERAMIC PACKAGES. MIL STD, 883B MAY BE SPECIFIED.

Nitron

NC5XXX SERIES CMOS GATE ARRAYS

NITROCHIP

GENERAL DESCRIPTION

Nitron's NC5XXX series CMOS Gate Array Family consists of seven (7) configurations as summarized in Table 1. Circuit complexities range from 50 equivalent two input gates to 600 equivalent gates (350 gates plus 72 dedicated flip flops).

These arrays are offered in standard plastic, ceramic, and cerdip dual-in-line packages. See Table 2. Lead count depends on array size and I/O utilization.

The arrays are based on groups of cells of three (3) and two (2) pairs of NMOS and PMOS transistors which are connected at the metal mask level to form CMOS logic and analog functions. Around the array cells are the bonding pads, input protection circuitry and driver and buffer cells.

FEATURES

- RELIABLE METAL GATE CMOS TECHNOLOGY
- LOW POWER OPERATION
- WIDE TOLERANCE OF OPERATION VOLTAGE AND TEMPERATURE
- FAST DESIGN CYCLE
- LOW DEVELOPMENT COST
- VOLUME PRODUCTION CAPABILITY
- SECOND SOURCE AVAILABLE

TABLE 1. NC5XXX SERIES CMOS GATE ARRAY FAMILY

Device	Equivalent Two Input Gates	Driver Cells	Buffer Cells	Bonding Pads	Alternate Sources
NC5050	50	10	18	22	ML 50
NC5100	100	14	30	32	ML 100 MCA
NC5150	150	18	32	38	ML 150 MCB
NC5200	200	18	44	44	ML 200 MCC
NC5350	200 + 32FF	16	60	53	ML 350 MCD
NC5500	450 + 24FF	20	84	84	FE 500
NC5600	350 + 72FF	20	84	84	FE 600

TABLE 2. NC5XXX SERIES CMOS GATE ARRAY PACKAGE OPTIONS

	PACKAGE					
Device	14 Pin	16 Pin	18 Pin	24 Pin	28 Pin	40 Pin
NC5050	YES	YES	YES	YES	YES	YES
NC5100	YES	YES	YES	YES	YES	YES
NC5150	NO/YES**	YES	YES	YES	YES	YES
NC5200	NO/YES**	YES*	YES*	YES	YES	YES
NC5350	NO	NO	NO	YES	YES	YES
NC5500	NO	NO	NO	YES	YES	YES
NC5600	NO	NO	NO	YES	YES	YES

OTHER PACKAGES ARE AVAILABLE AS REQUIRED.
*ORIENTATION MUST BE IN LINE WITH CAVITY.
**IN PLASTIC ONLY

The technology used for these products is NITRON'S 7 micro metal gate CMOS. This process offers all the conventional advantages of CMOS, i.e., very low power consumption, broad power supply ranges and high noise immunity. Typical array propagation delays are in the 13 to 5 ns range for VDD values of 5 to 15 volts.

ABSOLUTE MAXIMUM RATINGS (Non-operating) above which useful life may be impaired. All voltages are referenced to V_{SS}.

- Supply Voltage V_{DD} .... -0.5 to 18V
- Voltage on any Input .... -0.5 to V_{DD}+0.5V
- Current into any Input .... ±10mA
- Storage Temperature .... -65° C to 150° C
- Lead Temperature (Soldering, 10s) .... 300° C
- Operating Temperature -55° C to +125° C .... -55° C to +125° C

RECOMMENDED OPERATING CONDITIONS

NITRON CMOS will operate over a recommended V_{DD} power supply range of 3 to 15V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} equal to 5, 10 and 15V. Where low power dissipation is required, the lowest power supply voltage, consistent with required speed, should be used. For larger noise immunity, higher power supply voltages should be specified. Because of its wide operating range, power supply regulation and filtering are less critical than with other types of logic. The lower limit of supply regulation is 3V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15V or as determined by power dissipation constraints or interface to other logic.

DC CHARACTERISTICS: V_{DD} = 5V, V_{SS} = 0V

Symbol	Parameter	Limits			Units	Temp	Test Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	3.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			1.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	4.99 4.95			V	Min. 25° C Max	I_{OH} = 0mA, Inputs at 0 or 5V per the Logic Function or Truth Table
		4.0			V	All	I_{OH} = 0mA, Inputs at 1.5 or 3.5V
V_{OL}	Output LOW Voltage			0.01 0.05	V	Min. 25° C Max	I_{OL} = 0mA, Inputs at 0 or 5V per the Logic Function or Truth Table
				0.5	V	All	I_{OL} = 0mA, Inputs at 1.5 or 3.5V
I_{IN}	Input Current XC			0.1	µA	25° C	Lead under test at 0 or 5V All other Inputs Simultaneously at 0 or 5V
	XM			0.01			
I_{OH}	Output HIGH Current	-1.5 -1.0			mA	Min. 25° C Max	V_{OUT} = 2.5V; "Buffer" Output Inputs at 0 or 5V per the Logic Function or Truth Table
		-0.4 -0.2			mA	Min. 25° C Max	V_{OUT} = 4.5V
I_{OL}	Output LOW Current	0.7 0.6 0.4			mA	Min. 25° C Max	V_{OUT} = 0.4V
I_{OL}	Output LOW Current	3.0 2.5 1.6			mA	Min. 25° C Max	V_{OUT} = 0.4V; "Driver" Output
I_{IH}	Input HIGH Current			10	µA	Max	V_{IN} = V_{IH}
I_Z	Output Leakage Current			10	µA	Max	V_{OUT} = V_{DD}

DC CHARACTERISTICS: V_{DD} = 10V, V_{SS} = 0V

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Temp	Test Conditions
V_{IH}	Input HIGH Voltage	7.0			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			3.0	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	9.99 9.95			V	Min. 25° C Max	I_{OH} = 0mA, Inputs at 0 or 10V per the Logic Function or Truth Table
		9.0			V	All	I_{OH} = 0mA, Inputs at 3 or 7V
V_{OL}	Output LOW Voltage			0.01 0.05	V	Min. 25° C Max	I_{OL} = 0mA, Inputs at 0 or 10V per the Logic Function or Truth Table
				1.0	V	All	I_{OL} = 0mA, Inputs at 3 or 7V
I_{IN}	Input Current XC			0.1	µA	25° C	Lead under test at 0 or 10V All other Inputs Simultaneously at 0 or 10V
	Input Current XM			0.01			
I_{OH}	Output HIGH Current	-0.5 -0.3			mA	Min. 25° C Max	V_{OUT} = 9.5V; "Buffer" Output Inputs at 0 or 10V per the Logic Function or Truth Table
I_{OL}	Output LOW Current	1.3 1.0 0.6			mA	Min. 25° C Max	V_{OUT} = 0.5V; "Buffer" Output Inputs at 0 or 10V per the Logic Function or Truth Table
I_{OL}	Output LOW Current	5.0 4.0 2.5			mA	Min. 25° C Max	V_{OUT} = 0.5V; "Driver" Output

DC CHARACTERISTICS: V_{DD} = 15V, V_{SS} = 0V

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Temp	Test Conditions
V_{IH}	Input HIGH Voltage	10.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			4.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	14.99 14.95			V	Min. 25° C Max	I_{OH} = 0mA, Inputs at 0 or 15V per the Logic Function or Truth Table
		13.0			V	All	I_{OH} = 0mA, Inputs at 4.5 or 10.5V
V_{OL}	Output LOW Voltage			0.01 0.05	V	Min. 25° C Max	I_{OL} = 0mA, Inputs at 0 or 15V per the Logic Function or Truth Table
				2.0	V	All	I_{OL} = 0mA, Inputs at 4.5 or 10.5V
I_{IN}	Input Current XC			1.0	µA	25° C	Lead under test at 0 or 15V All other Inputs Simultaneously at 0 or 15V
	Input Current XM			1.0			
I_{OH}	Output HIGH Current	-1.4 -0.84			mA	Min. 25° C Max	V_{OUT} = 13.5V; "Buffer" Output Inputs at 0 or 15V per the Logic Function or Truth Table
I_{OL}	Output LOW Current	3.6 2.0			mA	Min. 25° C Max	V_{OUT} = 1.5V; "Buffer" Output Inputs at 0 or 15V per the Logic Function or Truth Table
I_{OL}	Output LOW Current	14.0 8.0			mA	Min. 25° C Max	V_{OUT} = 1.5V; "Driver" Output

AC CHARACTERISTICS: V_{DD} AS INDICATED, V_{SS} = 0V, T_A = 25° C

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	V_{DD}	Conditions
t_{PLH}	Array Cell Propagation Delay		13 7 5	20 11 8	ns ns ns	5.0V 10.0V 15.0V	Inverter, C_L = 1pF
t_{PHL}	Array Cell Propagation Delay		13 7 5	20 11 8	ns ns ns	5.0V 10.0V 15.0V	Inverter, C_L = 1pF
t_{TLH}	Output Transition Time		80 50 30	150 80 50	ns ns ns	5.0V 10.0V 15.0V	"Buffer" Output, C_L = 50pF
t_{THL}	Output Transition Time		80 50 30	150 80 30	ns ns ns	5.0V 10.0V 15.0V	"Buffer" Output, C_L = 50pF
t_{TLH}	Output Transition Time		13 7 5	80 50 30	ns ns ns	5.0V 10.0V 15.0V	"Buffer" Output, C_L = 15pF
t_{THL}	Output Transition Time		13 7 5	80 50 30	ns ns ns	5.0V 10.0V 15.0V	"Buffer" Output, C_L = 15pF
f_{MAX}	Maximum Clock Frequency	3.5 5 6.5	5 8 10		MHz MHz MHz	5.0V 10.0V 15.0V	Ripple Counter or Shift Register $C_L \leq$ 1pF

Typical temperature coefficient = 0.3%/°C   Input rise and fall times ≤ 20ns

R-10-81

SILICON GATE CMOS GATE ARRAY

NC9XXX

PRELIMINARY

Nitron

NITROCHIP

FEATURES

* Metal and Contact Mask programmable
* 360 to 1500 equivalent Gate Complexity
* Typical Gate propagation delay of 3-6 nsec
* 85 to 90 percent of Gate Utilization
* All outputs are TTL Compatible and Latch-up free
* High Output Sinking and Sourcing Capability
* Supported by predefined Macrocell Library
* Commercial and Military temperature ranges
* Second source available

DESCRIPTION

The NC9XXX series of Silicon Gate CMOS Arrays comprise a high performance family of six logic arrays, with complexity ranging from 360 to 1500 equivalent gates, and a maximum pincount ranging from 50 to 96. These devices are metal and contact masks programmable.

The NC9XXX series of Gate Arrays is manufactured using a proven Silicon Gate Oxide isolated CMOS process with a single layer of metal interconnect and a layer of contact, defining the logic function being implemented.

The circuits are organized as arrays of cells and I/O Buffers as shown in Fig. 1. The basic cell interconnected as a 2 input nand gate is shown in Fig. 2. The individual n-ch. and p-ch. transistors may be configured into a variety of SSI Logic elements called macrocells, using predefined contact and metal interconnections.

PRODUCT OUTLINE

PART NUMBER	EQUIV. GATES	MAX. PINS	GATE SPEED (MAX) NSEC	TTL OUTPUT BUFFERS	DESIGN TURN AROUND TIME (WEEK)
NC9360	360	52	5	50	8
NC9540	540	62	5	60	8
NC9720	720	70	5	68	10
NC9960	960	80	5	78	10
NC91200	1200	88	5	86	12
NC91500	1500	98	5	96	12

10420 Bubb Road, Cupertino, California 95014
Telephone (408) 255-7550 TWX 910-338-0222

OPERATING CHARACTERISTICS

Absolute Maximum Ratings (Referenced to V_{SS})

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	-0.5 to +12	V
Input Voltage	V_1	-0.5 to V_{DD} +5	V
DC Input Current	I_{IN}	+/- 10	mA
Storage Temperature Range (Ceramic)	T_{STG}	-65 to +150	°C
Storage Temperature (Plastic)	T_{STG}	-40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol		Unit
DC Supply Voltage	V_{DD}	+3 to +10	V
Operating Ambient Temperature Range			
Military	T_A	-55 to +125	°C
Industrial Range	T_A	-40 to + 85	°C
Commercial Range	T_A	0 to + 70	°C

AC CHARACTERISTICS

Specified at V_{DD} = 5V +/- 10% fanout of 2.

Macrocell	tPD nsec		
	Min.	Typ.[2]	Max.[3]
Inverter		2	3
2 -- Input NAND		3	5
2 -- Input NOR		3	5
3 -- Input NAND		5	10
3 -- Input NOR		6	10
4 -- Input NAND		8	15
4 -- Input NOR		9	17
D Flip-Flop [1]		10	20

Propagation delay (t_{PD}) =

$$\frac{t_{PLH} + t_{PHD}}{2}$$

Notes:

1. From Clock transition
2. At T_A = 25°C
3. At T_A = 70°C

DC CHARACTERISTICS -- TTL INTERFACE

Specified at V_{DD} + 5V +/- 10% and ambient temperature over the specified temperature range [1]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2[4]			V
I_{IL}	Low Level Input Current	$V_I = V_{SS}$	-10	-0.001	10	uA
I_{IH}	High Level Input Current	$V_I = V_{DD}$	-10	0.001	10	uA
V_{OH}	High Level Output Voltage TTL Buffer	I_{OH} = -3.0 mA	2.4	4.5		V
	LS Buffer	I_{OH} = 700 uA	2.7	4.5		V
V_{OL}	Low Level Output Voltage TTL Buffer	I_{OH} = 4.0 mA[3]		0.22	0.4	V
	LS Buffer	I_{OH} = 0.8 mA		0.22	0.4	V
I_{OZ}	Three State Output Leakage Current	V_{OH} = 0.0 V or 5.0 V	-10	±0.001	10	uA
I_{OS}	Short Circuit Output Current TTL Buffer	V_{OS} = 5.0 V			60	mA
		V_{OS} = 0.0 V			-25	mA
	LS Buffer	V_{OS} = 5.0 V			15	mA
		V_{OS} = 0.0 V			-7	mA

(See following page for notes)

DC CHARACTERISTICS -- CMOS INTERFACE

(EIA/JEDEC format for CMOS Industry B specifications)

Symbol	Parameter	Condition	VDD	T Low[1] Min.	T Low[1] Max.	25°C Min.	25°C Typ.	25°C Max.	T High[1] Min.	T High[1] Max.	Unit
I_{DD}	Quiescent Device Current	$V_I = V_{DD}$ or V_{SS}	5V		0.2		0.0002	0.2		2	uA/gate
			10V		0.4		0.005	0.4		4	uA/gate
V_{OL}	Low Level Output Voltage	I_O _ 1uA	All		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	I_O _ 1uA	5V	4.95		4.95			4.95		V
			10V	9.95		9.95			9.95		V
V_{IL}	Input Low Voltage		5V		1.5			1.5		1.5	V
			10V		3.0			3.0		3.0	V
V_{IH}	Input High Voltage		5V	3.5		3.5			3.5		V
			10V	7.0		7.0			7.0		V
I_{OL}	Output Low[2] (Sink Current) TTL Buffer	$V_O = 0.4V$	5V	3.2		3.2	4.8		2.4		mA
		$V_O = 2.5V$	5V	9.0			13.5		6.8		mA
		$V_O = 0.5V$	10V	6.0		6.0	9.1		4.0		mA
		$V_O = 5.0V$	10V	19.0			35.6		11.6		mA
	LS Buffer	$V_O = 0.4V$	5V	1.0		1.0	1.6		0.8		mA
		$V_O = 2.5V$	5V	3.0			4.0		2.0		mA
		$V_O = 0.5V$	10V	1.8		1.8	3.1		1.0		mA
		$V_O = 5.0V$	10V	6.0			9.0		3.0		mA
I_{OH}	Output High (Source Current) TTL Buffer	$V_O = 4.6V$	5V	0.6		0.6	1.5		0.5		mA
		$V_O = 2.5V$	5V	4.0			6.4		3.2		mA
		$V_O = 9.5V$	10V	1.1		1.1	3.0		0.9		mA
		$V_O = 5.0V$	10V	5.2			13.0		4.2		mA
	LS Buffer	$V_O = 4.6V$	5V	0.3		0.3	0.75		0.25		mA
		$V_O = 2.5V$	5V	2.0			3.1		1.6		mA
		$V_O = 9.5V$	10V	0.56		0.56	1.5		0.47		mA
		$V_O = 5.0V$	10V	2.8			6.7		2.1		mA
	Input Leakage Current	$V_{IN} = 0$ or V_{DD}	All		±0.1		±0.001	±0.1		±1.0	uA
	3 State Output Leakage Current	$V_O = 0$ or V_{DD}	All		± 1		±0.001	± 1		±10	uA
	Input Capacitance	Any Input	All				5				pF

Notes:

1. Military temperature range is -55°C to +125°C (ceramic packages only)
   Industrial temperature range is -40°C to +85°C
   Commercial temperature range is 0°C to +70°C
2. There may be limitations on maximum current when many outputs are low simultaneously
3. I_{OH} = 2.4 mA above +85°C
4. Using a TTL input buffer

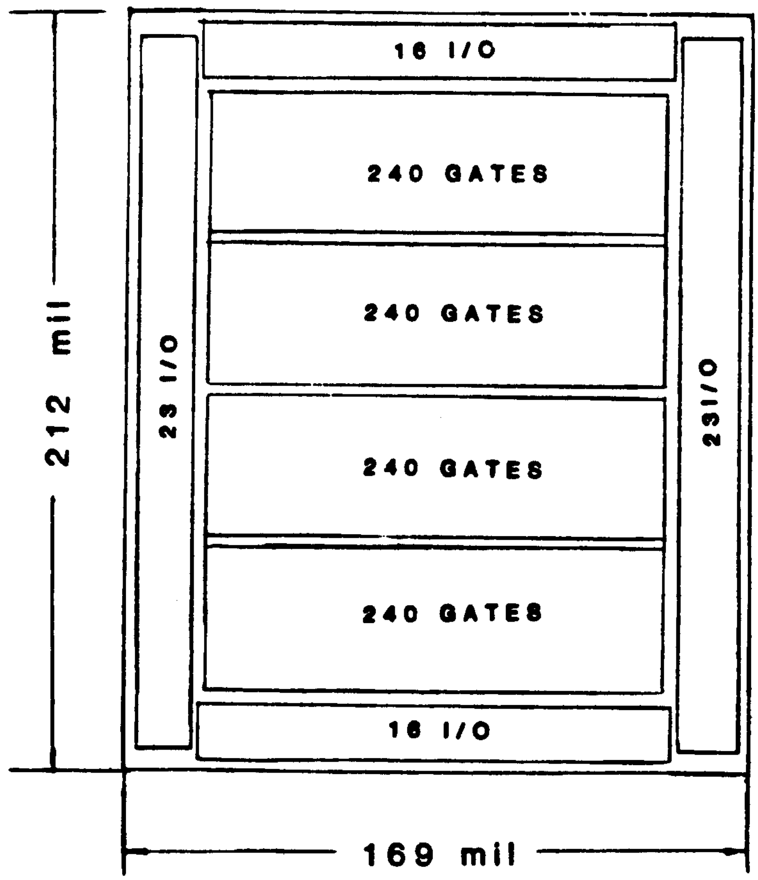


Fig. 1 - Chip Layout NC9960

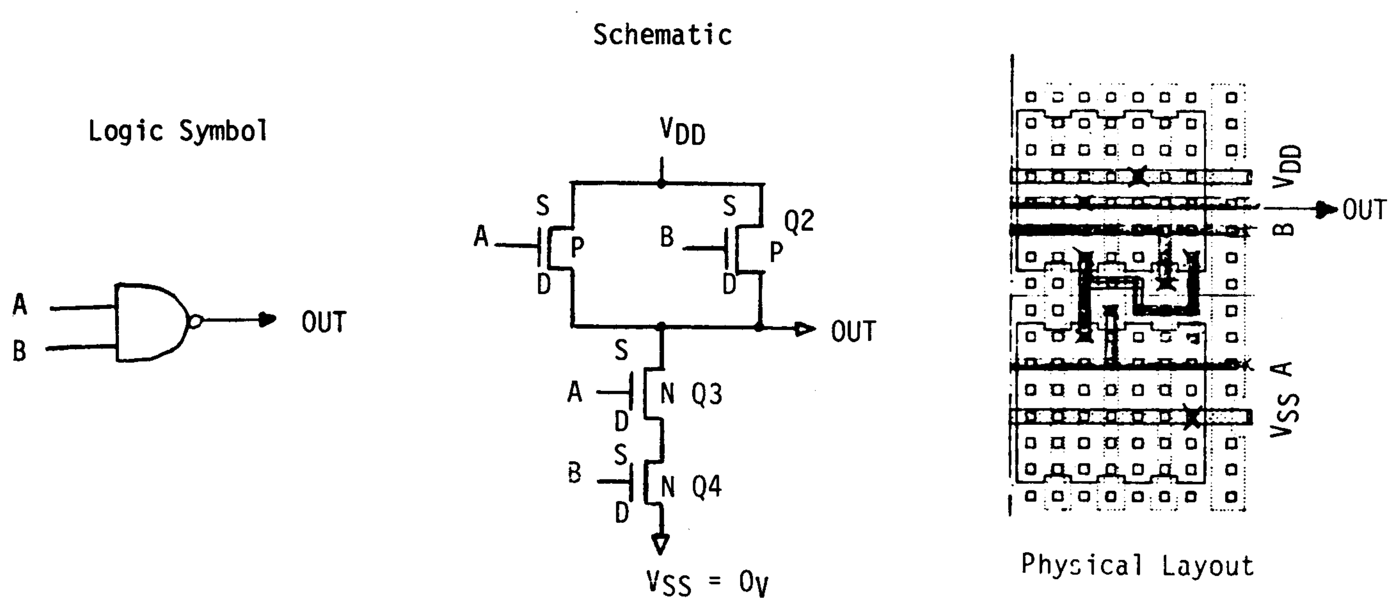


Fig. 2 - Basic Cell - Organized as 2 Input Nand Gate

BREADBOARDING

A well constructed and properly tested breadboard is a very useful tool for exposing documentation errors, design oversights marginal timing conditions or improper function of a digital circuit before it is committed to integration. Improvements and changes made at the breadboard stage can usually be checked out and documented in a few hours, whereas changes made after the integration is complete may take several weeks and be quite expensive. No matter how simple the digital circuit, it is suggested that a complete breadboard be built and evaluated before proceeding with the layout. The following guidelines should prove useful.

a) Use standard CMOS parts, building the breadboard as recommended.

b) Document the breadboard logic carefully, recording pin numbers and IC part numbers for future reference.

c) Record waveforms under proper operation at key circuit nodes.

d) Look for marginal timing conditions.

e) Develop a tentative test philosophy for the LSI circuit.

f) Record input waveforms where practical, including realistic allowances for noise. Keep both the breadboard and the documentation for reference in preparing test programs described in a later section.

g) Finalize the circuit specification. Determine worst case loading condition and document the extremes of temperature, voltage, current and timing that the LSI circuit must meet.

In following this procedure, the user and Nitron are assured of a high probability that the design will work the first time.

When the breadboard has been used to verify the design, the layout may begin.

SELECTION OF OPTIMUM NITROCHIP

The CMOS Monochip family is designed to accommodate a wide variety of applications. To take advantage of this flexibility, the user must choose the proper package size and chip size, and arrange the circuit layout on the chip for efficient interconnection. The following step-by-step procedure is intended to guide the beginner through these numerous choices, and permit him to arrive at a good layout on the first try.

Step 1 - Determine pin count and select package size

Step 2 - Simplify the logic circuit for the breadboard schematic

Step 3 - Estimate cell count and select the appropriate Nitrochip

Step 4 - Assign I/O pads

Step 5 - Assign logic blocks and detail gate placement using chip layout map

Step 6 - Detailed gate placement

Step 7 - Draw in detailed wiring layout

LAYOUT AIDS

Nitrochip layout is made straightforward through the use of the following design aids:

1. Design Manual - A document provided by Nitron which provides a thorough description of device characteristics and detailed design procedure.
2. Chip layout - A guide for cell placement to minimize number and length of interconnects.
3. Worksheet - A 200X drawing of the basic chip showing all cell connections.
4. Overlays - Stick-on patterns of 15 most popular logic functions for use with worksheets.

TESTING NITROCHIP

All production units of semi-custom ICs are 100% electrically tested and screened to mutually agreed test specifications, using one of Nitron's several computerized test systems. In addition, Nitron Quality Assurance Department performs an independent set of electrical tests on randomly selected samples of production units, prior to shipment, to assure conformity with Nitron's Acceptable Quality Level (AQL) standards.

NITRON'S TEST CAPABILITIES

Nitron can perform two basic types of tests for production ICs:

(1) parametric testing which measures a specific parameter value (normally current or voltage) and compares it against pre-established limits; (2) functional testing which applies a series of operating conditions and compares the circuit under test with a known good device. These two types of tests can be performed both as steady state (DC) or dynamic (AC) measurements. Although DC tests are easily implemented by automated testers, AC tests are usually difficult and expensive to perform in production.

Nitron has a complete computer-controlled IC test facility to provide 100% electrical testing of IC chips either in wafer form, using automated wafer-probe stations, or in dual-in-line package form, using automatic handlers. Nitron's test facility has several independent computer controlled test systems.

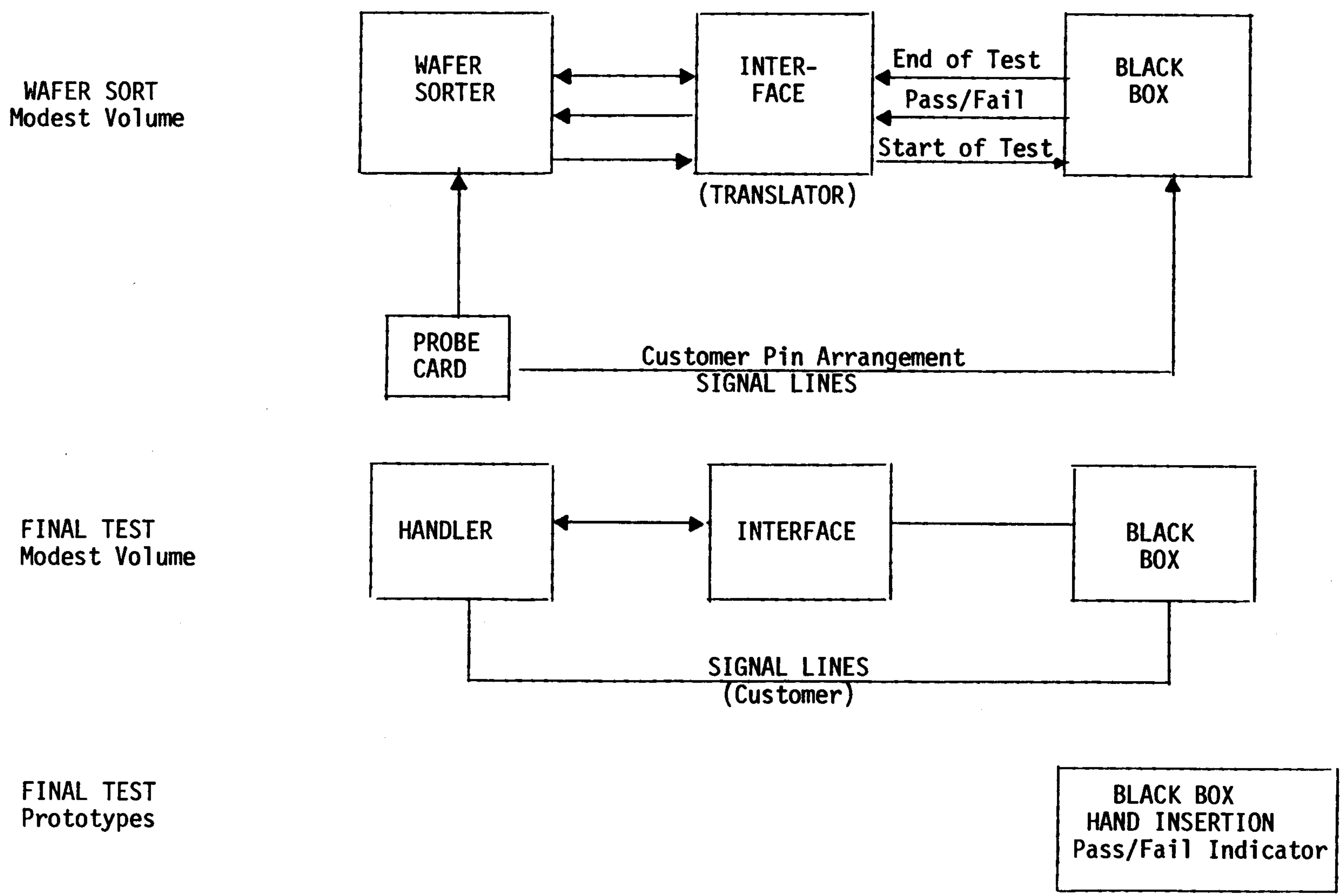
TEST INTERFACE DEVELOPMENT

Before releasing a semi-custom IC into production, it is necessary to develop a complete test interface (i.e., the necessary test program software and the interface hardware or fixtures) which will allow the monolithic chip to be 100% tested. This development effort normally requires four to six weeks to complete. However, it can be initiated in parallel with the IC development if a test plan is completed and a production commitment is made at the start of the program. There is normally a non-recurring engineering charge associated with this test interface development. This charge varies depending on the device specifications, test complexities and the follow-on production requirements. This charge is identified as part of the initial program development charge.

The general test interface is shown below which describes the arrangement used for testing prototypes and low to modest production volume. In each case, the device, in either wafer or package form, is tested using a "black box" which simulates the actual system environment, modified to permit rework location of the device under test (when a handler or wafer probe station is used) or to permit hand insertion of the device under test during prototype evaluation. In this latter case the black box alone is used and is provided with test switches and pass/fail indicators.

When the annual production volume is sufficient, the black box is replaced by one of the Computer controlled testers.

NITROCHIP GATE ARRAY TESTING



NITRON QUALITY ASSURANCE PROGRAM

The commitment of Nitron to Hi-Rel quality assurance standards began with the company's founding as a supplier to a major aerospace and military systems contractor. Since that time, Nitron has become a major supplier of Hi-Rel products to programs supporting all branches of military service. Our track record in this area is outstanding and our list of Hi-Rel customers is growing steadily.

Nitron's Quality Assurance standards comply with the major military specifications listed below, but is not limited to them. The company is participating in major custom programs which incorporate qualification and preconditioning testing of various part types. These standards are applied routinely to Nitron's semi-custom gate array product family.

TYPICAL MILITARY SPECIFICATIONS

Quality Program System	MIL-Q-9858A
General Specifications for Microcircuits (on a program basis)	MIL-M-38510
Inspection System Requirements	MIL-1-45208
Test Methods and Procedures	MIL-STD-883

The effect of these multiple quality assurance programs at Nitron is to provide military and commercial customers with documented, proven-quality LSI components.

100% ENVIRONMENTAL AND ELECTRICAL LOT SCREENING

The purpose of this screen is to assure a high level of quality and reliability within a lot of semiconductor devices. Nitron offers a wide range of Hi-Rel flow alternatives. This fact allows a user to select a Nitron standard flow or create, through the use of a drawing, a custom made screening program to exactly fit his individual needs. Nitron Product Engineering and Quality Groups often assist the user with the development of this documentation.

QUALITY CONFORMANCE AND QUALIFICATION

Nitron maintains ongoing reliability evaluations per MIL-STD-883 Method 5005, Class B, Groups B, C, and D. Mean life evaluation data is obtained by selecting random samples of product on a periodic basis and subjecting them to operating life tests. Failure analysis is performed on all confirmed rejects to assure the results are peninent and provide timely corrective action. Summary life test data accumulated on Nitron devices is available on request.

BENEFITS OF HI-REL SCREENING

- o Increased system reliability
- o Reduced system down time
- o Reduced in-house and field repair costs
- o Reduced customer dissatisfaction
- o Reduced inspection costs
- o User screening programs not necessary

NITRON 883 SCREENING PROGRAMS

REQUIREMENT	Method 5004 CLASS S	CLASS B	Nitron Standard Flow CLASS C
1 Internal Visual (Precap)	2010A	2010B	2010B
2 Stabilization Bake	X	X	X
3 Temp. Cycle and/or Thermal Shock	X	X	X
4 Constant Acceleration	X	X	X
5 Particle Impact Noise Detection	X	–	–
6 Seal (Fine & Gross)	OPT	X	X
7 Serialization	X	–	–
8 Interim Electrical	X	–	–
9 Burn-In	240HR	160HR	–
10 Interim Electrical	X	–	–
11 Reverse Bias Burn-in	72HR	–	–
12 Interim Electrical	X	X	–
13 Seal (Fine & Gross)	X	–	–
14 Final Electrical	X	X	X
15 Radiographic	X	–	–
16 External Visual	X	X	X

Extensive life testing has been performed at Nitron on CMOS metal gate devices identical in process and construction to the Nitrochip. The following tabulation shows the results of life testing such parts in cerdip packages over a 9 month period ending April 1981.

Test temp	Sample size	Device hours	Equiv device hrs at 55°C	FR %/K hrs 60% confidence at 55°C
150	495	247.5×10^3	34.7×10^1	0.006

Details of this life test program are found in Nitron Reliability Report "Low Power Metal Gate CMOS Process", dated August 1981.

USER QUESTIONNAIRE

Dear Nitron:

Please send me a budgetary quotation based on the following information:

FILL IN OR CIRCLE FOR ALL QUESTIONS

Maximum Clock Frequency:			________
Operating Temperature Range			°C to °C
Preliminary Circuit Diagram:	Included		Not Included
or			
Approximate Gate Count:			________
Pin Count:			________
Production Package:	Plastic	Cerdip	Ceramic
Temperature Testing Required:	Hot	Cold	No
High Reliability Screening:		Yes	No
Burn-In:		Yes	No
Date Contract to be Let:			________
Number of Units to be Purchased Annually:			________
Date Proto Units are Required:			________
Have an Applications Engineer Call:		Yes	No

Other Important Specifications or Comments:

____

____

____

NAME ____

POSITION ____

COMPANY ____

COMPANY ADDRESS ____

____

____

TELEPHONE ____

Send to Nitron Marketing 10420 Bubb Road Cupertino, Ca. 95014

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DELTA COMPONENTS
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Dallas, TX 75220
TEL: (214) 358-4288
TWX: 910-861-4248

NORTHERN CALIFORNIA
PACIFIC ELECTRONICS
548 Division Street
Campbell, CA 95008
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TLX: 172760

SOUTHERN CALIFORNIA
RELCOM, INC.
20335 Ventura Blvd.
Suite 203
Woodland Hills, CA 91365
TEL: (213) 340-9143
TWX: 910-494-4961

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LITTLEFIELD & SMITH ASSOC.
11772 Sorrento Valley Road
Suite 235
San Diego, CA 92121
TEL: (714) 455-0055
TWX: 910-322-1730

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COMPONENT SALES, INC.
5925 East Evans Avenue
Suite 204B
Denver, CO 80222
TEL: (303) 759-1666
TWX: 910-931-2644

CONNECTICUT
DATCOM, INC.
1 Evergreen Avenue
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TEL: (203) 288-7005
TWX: 92-3462

DELAWARE
JADE ELECTRONICS ASSOC., INC.
Hollow Road
Birchrunville, PA 19421
TEL: (215) 296-3800

FLORIDA
LAWRENCE ASSOCIATES, INC.
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TWX: 810-853-0260

Branch Office
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Clearwter, FL 33515
TEL: (813) 443-2698

Branch Office
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TEL: (505) 368-7373

Branch Office
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DIMARK
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Suite C
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TEL: (615) 639-0113 .

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COMPONENT SALES
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(Branch Office)
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TWX: 92-3462

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TEL: (317) 842-5203

(Northern)
INSUL-REPS, INC.
5618 Coldwater Road
Fort Wayne, IN 46825
TEL: (219) 482-1596
TWX: 810-332-1566

IOWA
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GREINER ASSOCIATES
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Minneapolis, MN 55441
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RELCOM, INC.
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Reno
PACIFIC ELECTRONICS
548 Division Street
Campbell, CA 95008
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NEW HAMPSHIRE
DATCOM, INC.
1 Evergreen Avenue
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NEW MEXICO
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